SD93F115

20 bits ADC with LCD driver 32 bits MCU SOC

Features

- High precision ADC, 18.6bits ENOB at 8sps (Gain = 256). It can be set to 4 differential or 8 single-ended inputs
- Low noise, high input impedance preamplifier with offset calibration and selectable gain options: 1, 4, 8, 16, 32, 64, 128 or 256
- 12 bits SAR ADC with self-calibration function. Sampling rate and operation mode are selectable
- 32 bits MCU, 120k Bytes Flash, 8k Bytes Boot and 8k Bytes SRAM
- Internal 24MHz and 32kHz RC oscillator with ±1% typical error after calibration
- RTC module with external 32.768kHz crystal provides calendar/time information, including leap year. Timing accuracy is adjustable.
- 33SEG x 4COM, 32SEG x 5COM, 31SEG x 6COM, 29SEG x 8COM LCD drives with ultra-low power consumption and high driving capability. The IC has a programmable boost module to maintain luminance at low supply voltage. Drive voltage range: 2.7~5.2V
- Built-in sensor excitation output. Voltage is 2.4~4.5V at 0.3V step
- Built-in burnout detect current source
- 1.2V benchmark output
- Built-in sine wave generator with selectable output frequency at 5kHz, 50kHz, 100kHz, and 200kHz. It supports an 8-electrode BIA fat measurement
- Two operational amplifiers: OPA and OPB
- Flexible low voltage detection and touch button detection circuits including an 8bits DAC and a rail-to-rail input comparator. The voltage detection range is 2.0~5.3V
- Built-in silicon temperature sensor with single-point correction, automatic forward and reverse measurement
- Peripheral resources include: UART, I2C, SPI, PWM/PDM, CCP, TIMER, Buzzer, 2 external interrupts, and 7 key interrupts
- All I/O have Schmidt trigger inputs and pull-up resistors. The resistance of the pull-up resistor is 50kΩ
- Operating voltage range: 2.4~5.5V
- Operating temperature range: -40~85℃

Description

The SD93F115 is a 32 bits MCU CMOS SoC with built-in high precision 24 bits ADC, LCD driver, and 120k bytes flash program memory.

The 32bits system can be read by byte, half word (16 bits), and full word (32 bits). When the power is on the system clock is 12MHz by default. Different frequencies can be selected through register configuration. The maximum frequency is 24MHz.

Four working modes are provided so users can select the optimum choice between speed and power. The modes are: normal, standby (WAIT), sleep (DOZE), and deeply sleep (STOP).

Applications

Sphygmomanometers, body weight scales, blood glucose meters and infrared temperature measurement.

Ordering Information

Product model	Encapsulation	Package
SD93F115-JQS	LQFP100	Tray Pack
SD93F115-JBS	LQFP64	Tray Pack
SD93F115-D	DICE	Box-packed

Comparison of main resources

Table 1. SD93F115 resources Comparison table

Model	Flash (Bytes)	SRAM (Bytes)	High precision ADC	SAR ADC	LCD	Timer	BUZ	External interrupt	RTC	I2C	SPI	UART	PWM/ PDM	Encapsulation information
SD93F115-JQS	120K	8K	Have	Have	4*44	T0/1/2	2	2	Have	1	1	2	2	LQFP100
SD93F115-JBS	120K	8K	Have	Have	4*34	T0/1/2	1	2	Have	1	1	1	2	LQFP64
SD93F115-D	120K	8K	Have	Have	4*44	T0/1/2	2	2	Have	1	1	2	2	DICE

Pin Diagram and Descriptions

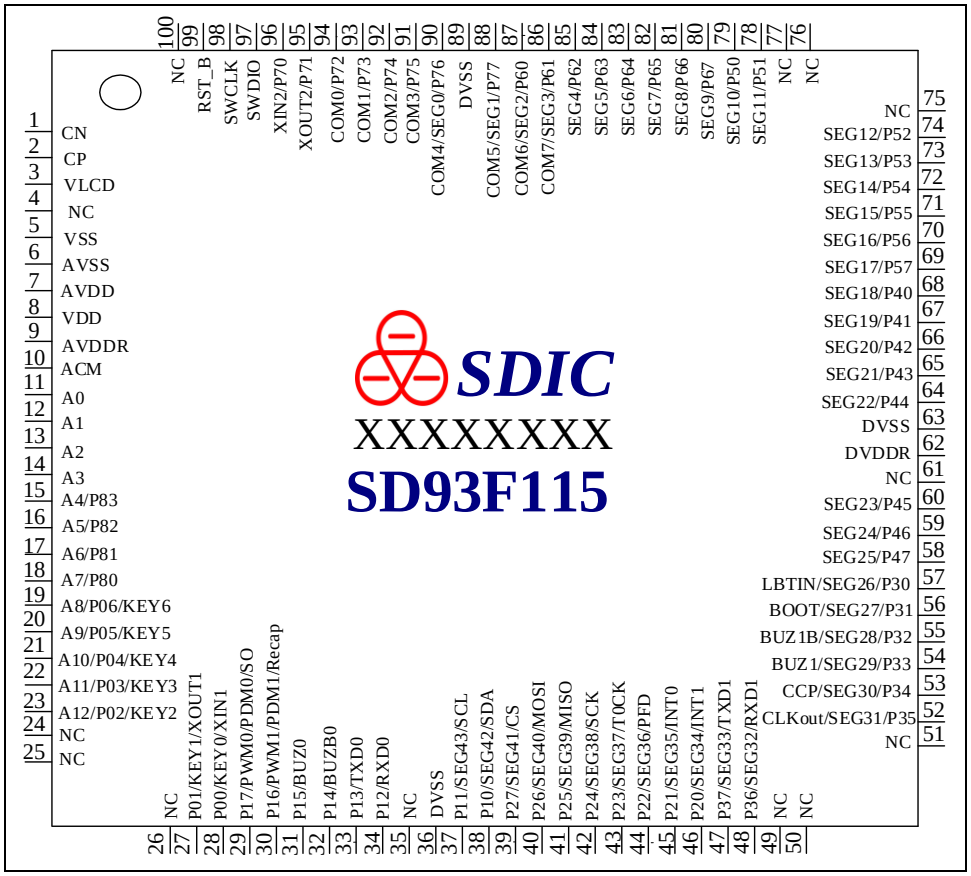


Figure 1. SD93F115-JQS Pad diagram（LQFP100）

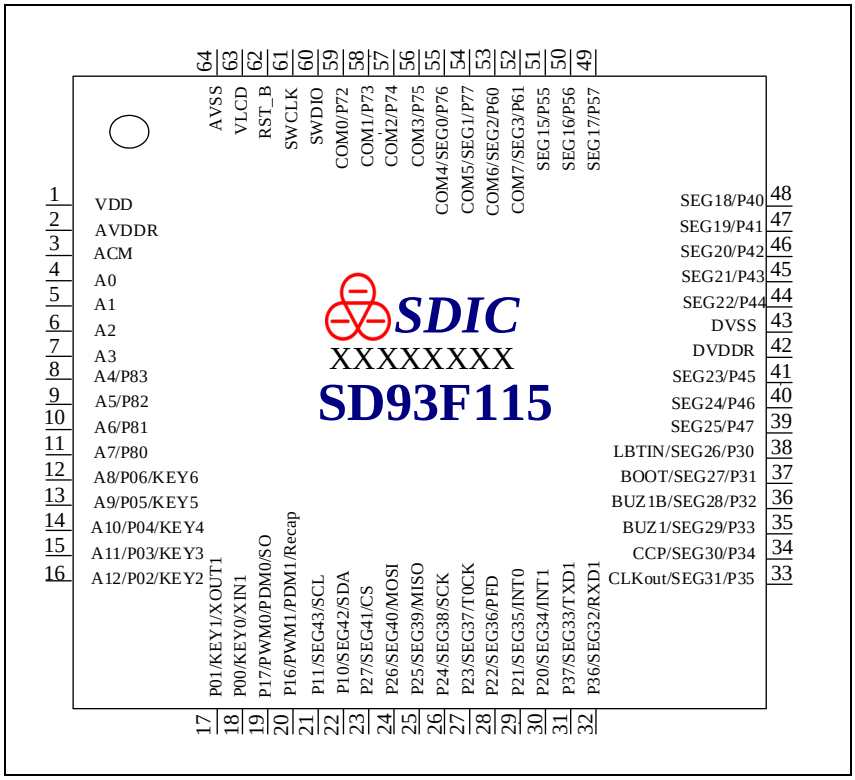


Figure2. SD93F115-JBS Pad diagram（LQFP64）

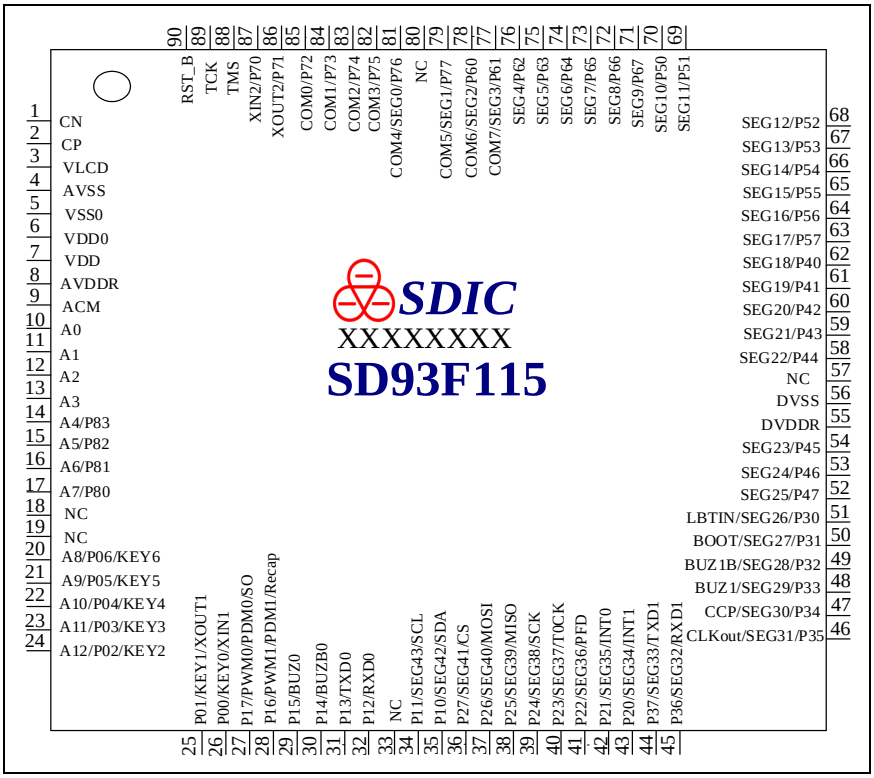


Figure3. SD93F115-D Pad diagram（DICE）

Table 2. Pin Descriptions

Pad No. Encapsulation 100 LQFP	Pad No. Encapsulation 64 LQFP	Pad No. Encapsulation DICE	Pin Name	Attribute	Description
1		1	CN	Analog	The boost circuit is externally connected with a capacitor pin , which can be externally connected with a capacitor of 0.1μF
2		2	CP		
3	63	3	VLCD	Analog	LCD driver power supply is internally connected to VDD or booster output through register setting. It connects 1μF filter capacitor to VDD
4			NC	NC	Please Keep it suspended and do not connect any external circuit
5	64	4	VSS	ground	ground
6		5	AVSS	Analog ground	Analog ground
7		6	AVDD	Analog Power	Internal LDO output for IC's analog module can provide excitation to the external transducer. It connects 0.1μF capacitor to VSS
8	1	7	VDD	Power	Power supply for the IC connects 0.1μF capacitor to AVSS
9	2	8	AVDDR	Analog	Internal LDO output for IC's analog module can provide excitation to the external transducer. It connects 0.1μF capacitor to VSS
10	3	9	ACM	Analog	1.2V reference output, floating when ACM is shutdown. It connects 0.1μF cap to AVSS
11	4	10	A0	Analog input	Analog signal inputs A0-3, can be used as 2 differential or 4 single-ended inputs. When not in use, each port should be pulled down to ACM by the register
12	5	11	A1		
13	6	12	A2		
14	7	13	A3		
15	8	14	A4/P83	Analog , I/O	Analog signal inputs A4-7 can be used as 2 differential or 4 single-ended inputs, or digital ports P83-P80
16	9	15	A5/P82		
17	10	16	A6/P81		
18	11	17	A7/P80		
		18	NC	NC	Please Keep it suspended and do not connect any external circuit
		19	NC	NC	Please Keep it suspended and do not connect any external circuit
19	12	20	A8/P06/KEY6	Analog , I/O	Analog signal inputs A8-12, digital ports P06-02, or external key inputs KEY6-2
20	13	21	A9/P05/KEY5		
21	14	22	A10/P04/KEY4		
22	15	23	A11/P03/KEY3		
23	16	24	A12/P02/KEY2		
24			NC	NC	Please Keep it suspended and do not connect any external circuit
25			NC	NC	Please Keep it suspended and do not connect any external circuit
26			NC	NC	Please Keep it suspended and do not connect any external circuit
27	17	25	P01/KEY1/XOUT1	Analog , I/O	Digital port P01, external key input KEY1, or 1~4MHz crystal oscillator pins
28	18	26	P00/KEY0/XIN1	Analog , I/O	Digital port P00, external key input KEY0, or 1~4MHz crystal oscillator pins XIN1
29	19	27	P17/PWM0/PDM0/ SO	Analog , I/O	Digital port P17, PWM0/PDM0 output, or sine wave output SO
30	20	28	P16/PWM1/PDM1/ Recap	Analog , I/O	Digital port P16, PWM1/PDM1 output, or rectifier circuit Recap output pin
31		29	P15/BUZ0	I/O	Digital port P15 , or BUZ0 output
32		30	P14/BUZB0	I/O	Digital port P15 , or BUZB0 output
33		31	P13/TXD0	I/O	Digital port P15 , or UART0 data transmits TXD0

Pad No.			Pin Name	Attribute	Description
Encapsulation					
100 LQFP	64 LQFP	DICE			
34		32	P12/ RXD0	I/O	Digital port P15 , or UART0 data receives RXD0
35			NC	NC	Please Keep it suspended and do not connect any external circuit
36		33	DVSS	Digital ground	Digital ground (if the bare chip is bonded , do not bond this pin , which is easy to damage the chip)
37	21	34	P11/SEG43/SCL	I/O	Digital port P11, LCD segment SEG43, or I2C clock signal
38	22	35	P10/SEG42/SDA	I/O	Digital port P10, LCD segment SEG42, or I2C digital signal
39	23	36	P27/SEG41/CS	I/O	Digital port P27, LCD segment SEG41, or SPI chip select signal CS
40	24	37	P26/SEG40/MOSI	I/O	Digital port P26, LCD segment SEG40, or data pin MOSI of SPI
41	25	38	P25/SEG39/MISO	I/O	Digital port P25, SEG39, or data pin MOSI of SPI
42	26	39	P24/SEG38/SCK	I/O	Digital port P24, SEG38, or SPI clock signal SCK
43	27	40	P23/SEG37/T0CK	I/O	Digital port P23, LCD segment SEG37, or TIMER0 external clock input T0CK
44	28	41	P22/SEG36/PFD	I/O	Digital port P22, LCD segment SEG36, or programmable frequency divider PFD
45	29	42	P21/SEG35/INT0	I/O	Digital port P21, LCD segment SEG35, or external interrupt INT0
46	30	43	P20/SEG34/INT1	I/O	Digital port P20, LCD segment SEG34, or external interrupt INT1
47	31	44	P37/SEG33/TXD1	I/O	Digital port P37, LCD segment SEG33, or UART1 data transmits TXD1,also can do burning interface TXD1
48	32	45	P36/SEG32/RXD1	I/O	Digital port P36, LCD segment SEG32, or UART1 data receives RXD1,also can do burning interface RXD1
49			NC	NC	Please Keep it suspended and do not connect any external circuit
50			NC	NC	Please Keep it suspended and do not connect any external circuit
51			NC	NC	Please Keep it suspended and do not connect any external circuit
52	33	46	P35/SEG31/CLKout	I/O	Digital port P35, LCD segment SEG31, or internal clock output CLKout
53	34	47	P34/SEG30/CCP	I/O	Digital port P34, LCD segment SEG30, or compare/capture output CCP
54	35	48	P33/SEG29/BUZ1	I/O	Digital port P33, LCD segment SEG29, or buzzer BUZ1 output
55	36	49	P32/SEG28/BUZ1B	I/O	Digital port P32, LCD segment SEG28, or buzzer BUZ1B output
56	37	50	P31/SEG27/BOOT	I/O	Digital port P31, LCD segment SEG27, or boot up area selection,also can do burning interface BOOT
57	38	51	P30/SEG26/LBTIN	Analog , I/O	Digital port P30, LCD segment SEG26, or low battery detect for LBTIN input
58	39	52	P47/SEG25	I/O	Digital port P47, LCD segment SEG25
59	40	53	P46/SEG24	I/O	Digital port P46, LCD segment SEG24
60	41	54	P45/SEG23	I/O	Digital port P45, LCD segment SEG23
61			NC	NC	Please Keep it suspended and do not connect any external circuit
62	42	55	DVDDR	Analog	Internal LDO output with typical value at 1.5V. It connects 0.1μF capacitor to ground
63	43	56	DVSS	Digital ground	Digital ground
		57	NC	NC	Please Keep it suspended and do not connect any external circuit

Pad No.			Pin Name	Attribute	Description
Encapsulation					
100 LQFP	64 LQFP	DICE			
64	44	58	P44/SEG22	I/O	Digital ports P44-40, LCD segments SEG22-18
65	45	59	P43/SEG21		
66	46	60	P42/SEG20		
67	47	61	P41/SEG19		
68	48	62	P40/SEG18		
69	49	63	P57/SEG17	I/O	Digital ports P57-56, LCD segments SEG17-16
70	50	64	P56/SEG16		
71	51	65	P55/SEG15	I/O	Digital ports P55-52, LCD segments SEG15-12
72		66	P54/SEG14		
73		67	P53/SEG13		
74		68	P52/SEG12		
75			NC	NC	Please Keep it suspended and do not connect any external circuit
76			NC	NC	Please Keep it suspended and do not connect any external circuit
77			NC	NC	Please Keep it suspended and do not connect any external circuit
78		69	P51/SEG11	I/O	Digital ports P51-50, LCD segments SEG11-10
79		70	P50/SEG10		
80		71	P67/SEG9	I/O	Digital ports P67-62, LCD segments SEG9-4
81		72	P66/SEG8		
82		73	P65/SEG7		
83		74	P64/SEG6		
84		75	P63/SEG5		
85		76	P62/SEG4		
86	52	77	P61/COM7/SEG3	I/O	Digital port P61, LCD COM7, or LCD segments SEG3
87	53	78	P60/COM6/SEG2	I/O	Digital port O P60, LCD COM6, or LCD segments SEG2
88	54	79	P77/COM5/SEG1	I/O	Digital port P77, LCD COM5, or LCD segments SEG1
89		80	DVSS	Digital ground 2	Digital ground(if the bare chip is bonded , do not bond this pin , which is easy to damage the chip)
90	55	81	P76/COM4/SEG0	I/O	Digital port P76, LCD COM4, or LCD segments SEG0
91	56	82	P75/COM3	I/O	Digital port P75-72, LCD COM3-0
92	57	83	P74/COM2		
93	58	84	P73/COM1		
94	59	85	P72/COM0		
95		86	P71/XOUT2	Analog , I/O	Digital port P71, or UART2 data transmits TXD2
96		87	P70/XIN2	Analog , I/O	Digital port P70, or UART2 data receives RXD2
97	60	88	SWDIO	I/O	SWD digital I/O
98	61	89	SWCLK	I/O	SWD clock input
99	62	90	RST_B	Analog	External reset, active low with internal pull-up
100			NC	NC	Please Keep it suspended and do not connect any external circuit

Remark:

1、 All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.

2、 If DICE bare chip bond, Pin33 and Pin80 DVSS pin don't bond, easy to damage the chip.

Functional Block

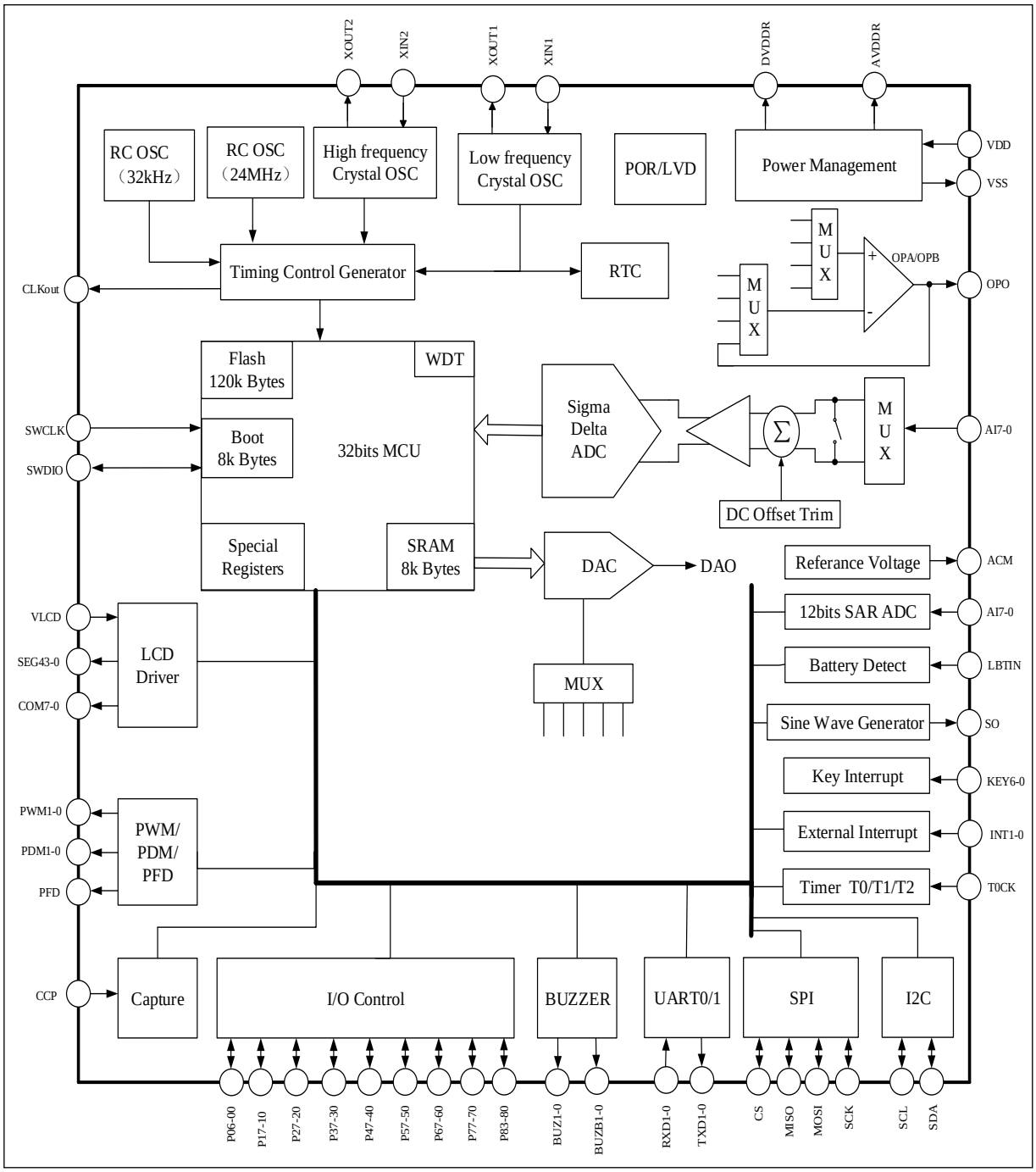


Figure 4. Functional block diagram

Typical Applications

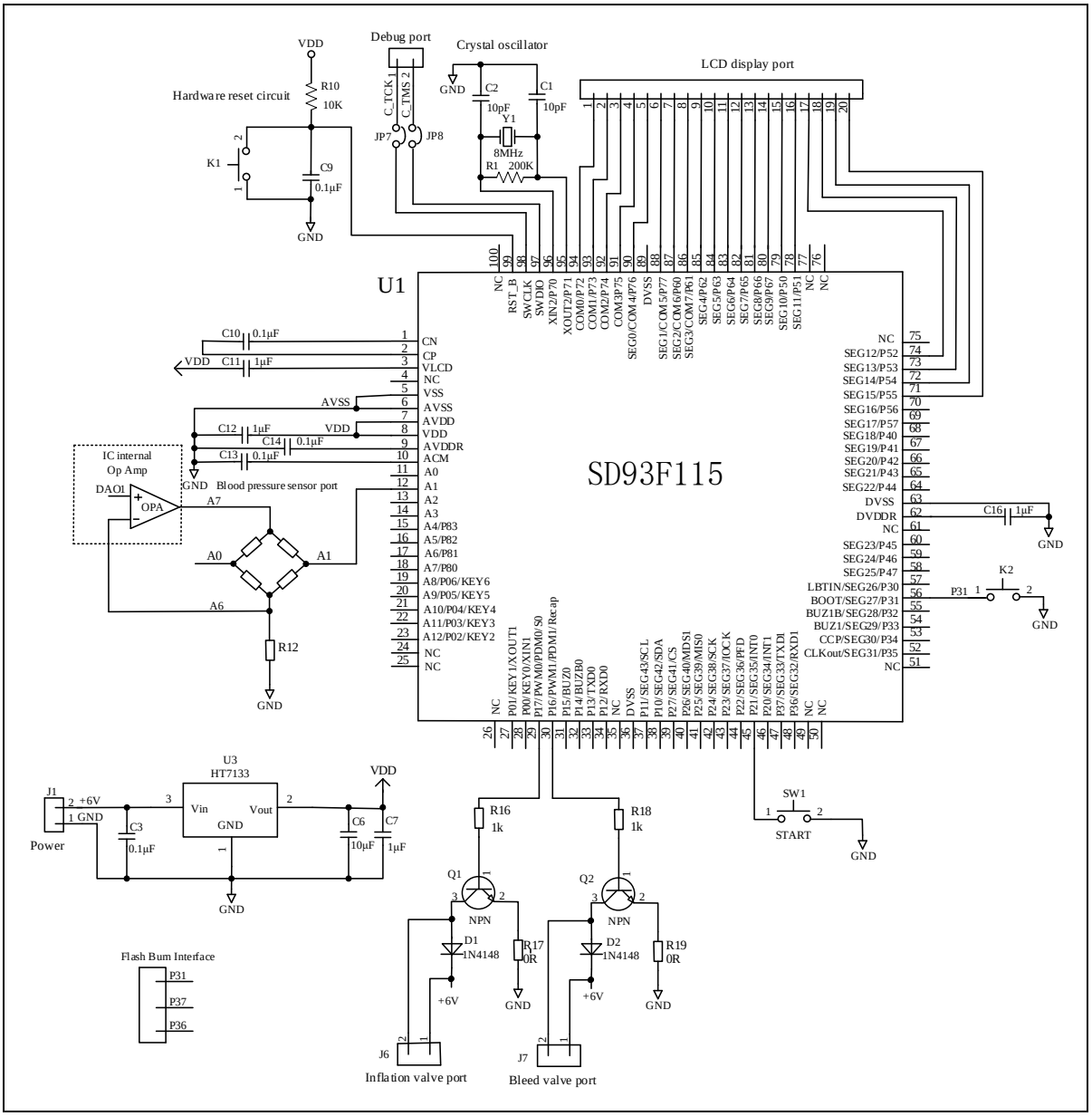


Figure 5. Typical application diagram of SD93F115-JQS Sphygmomanometer

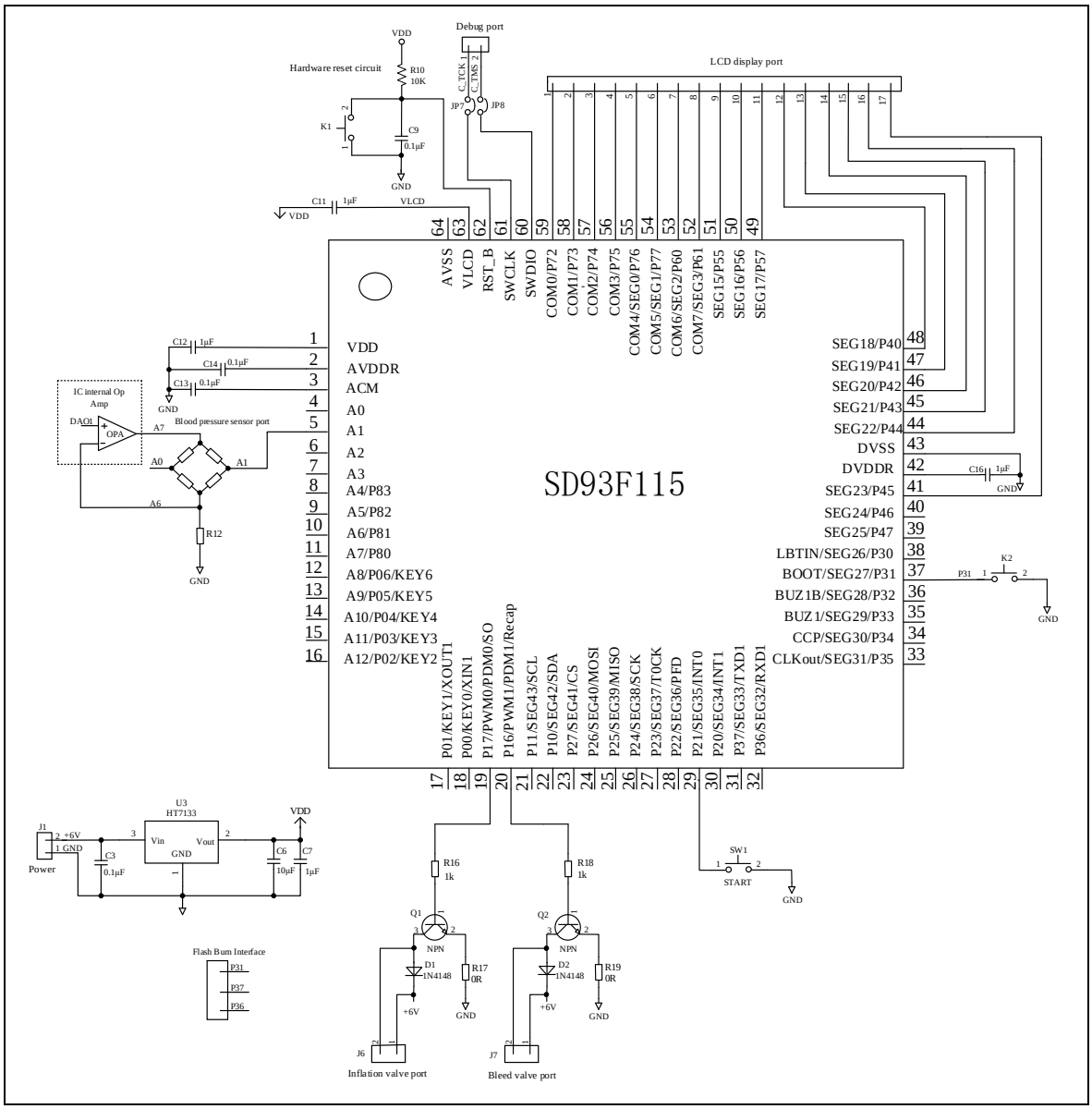


Figure 6. Typical application diagram of SD93F115-JBS Sphygmomanometer

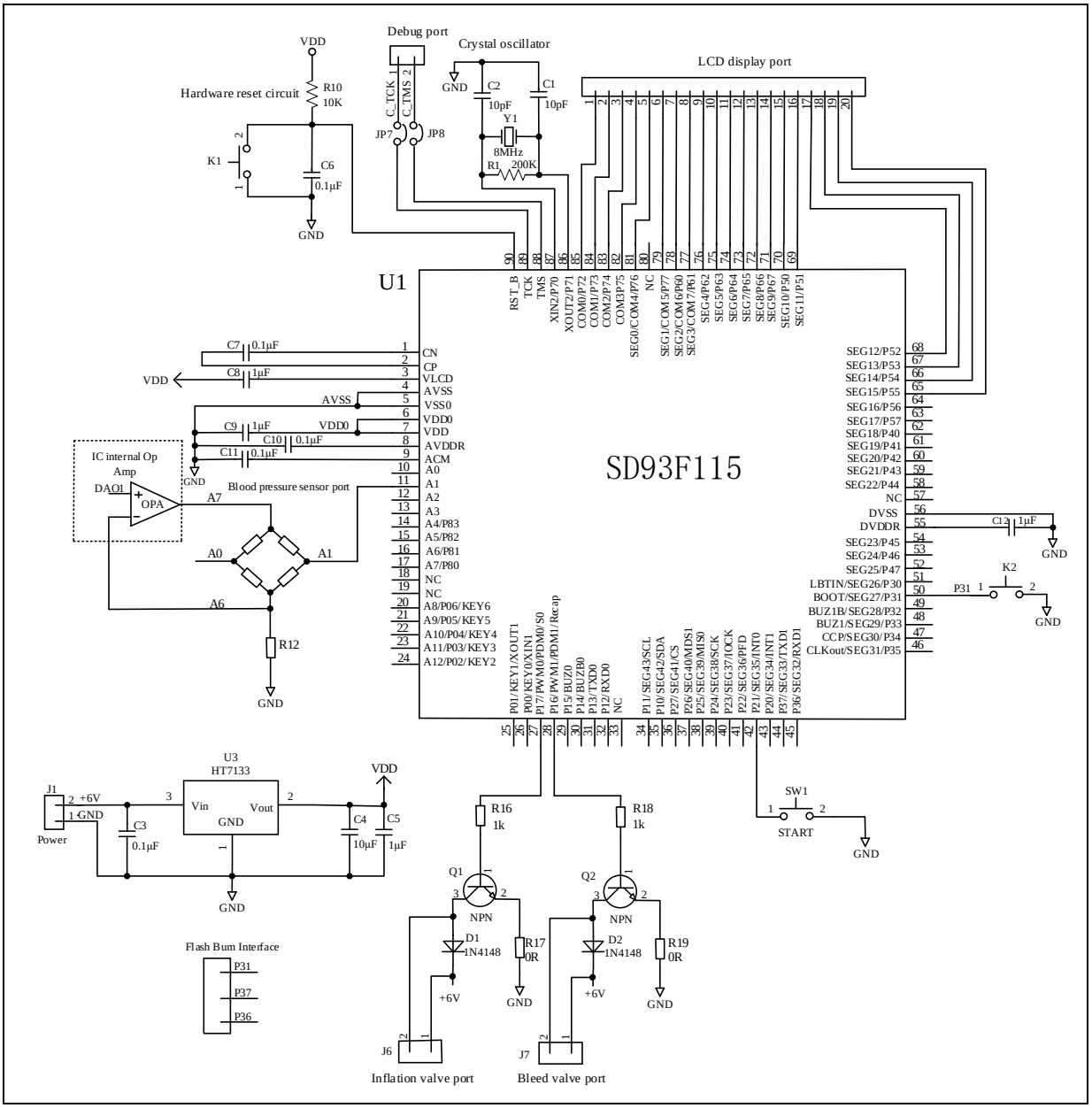


Figure 7. Typical application diagram of SD93F115-JBS Sphygmomanometer

ADC Characteristics

Table 3. ENOB and voltage noise Vn_{rms}
(AVDDR = 2.4V, VREF = AVDDR , SINC3 , Buffer、 Chopper on , fb > fh > fl ≥ fs/OSR, IAD = 1)

ADC sampling rate = 250kHz								
OSR		256	512	1024	2048	4096	8192	16384
256	ENOB	15.5	16.1	16.6	17.1	17.6	18.1	18.6
	Vn_{rms}(nV)	396.4	260.8	182.5	129.0	92.3	64.8	46.0
128	ENOB	16.3	17.0	17.5	18.0	18.5	19.0	19.5
	Vn_{rms}(nV)	475.4	289.9	198.5	138.3	99.8	69.4	48.5
1	ENOB	17.0	18.1	18.8	19.4	19.8	20.5	21.0
	Vn_{rms}(nV)	37205.8	16895.2	10506.0	6664.4	5641.7	3271.5	2306.1

ADC sampling rate = 750kHz								
OSR		256	512	1024	2048	4096	8192	16384
256	ENOB	15.3	15.9	16.4	16.9	17.4	17.9	18.4
	Vn_{rms}(nV)	451.8	309.6	216.5	152.7	107.5	75.4	55.2
128	ENOB	16.1	16.7	17.2	17.7	18.2	18.8	19.3
	Vn_{rms}(nV)	536.7	347.2	243.3	172.0	121.4	84.0	59.6
1	ENOB	17.0	18.1	18.8	19.4	19.9	20.4	21.0
	Vn_{rms}(nV)	37079.3	17522.1	10591.7	7140.6	4892.4	3378.2	2339.3

Remark:

1. The above data are averages based on multiple ICs' measured results. Each IC contributes 1024 data points.
2. ENOB = $\log_2(\frac{FRS}{Vrms})$, FRS is the Full-Scale Voltage Range (2 * Vref / Gain), Vrms is the rms Noise.
3. fb is the buffer chopping frequency. fl is the PGIA external chopping frequency. fh is the PGIA internal chopping frequency. IAD is the PGIA operating mode option.

Oscillator Characteristics

Figure 8 and figure 9 are SD93F115 oscillating frequency as a function of power supply voltage from five parts.

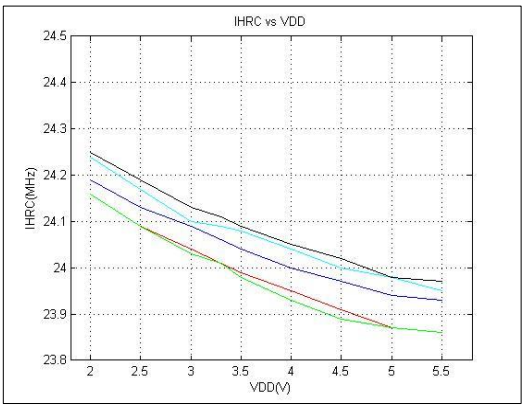


Figure 8. IHRC frequency vs voltage

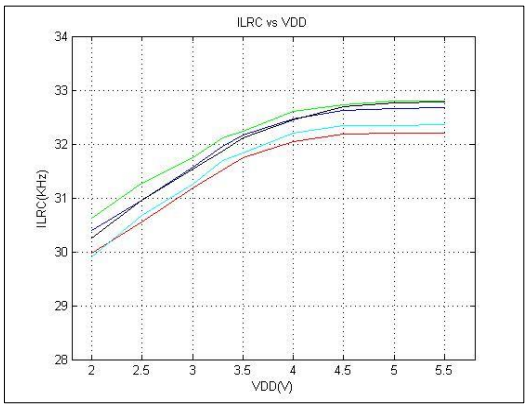


Figure 9. ILRC frequency vs voltage

Figure 10 and figure 11 are SD93F115 oscillating frequency as function of temperature from five parts.

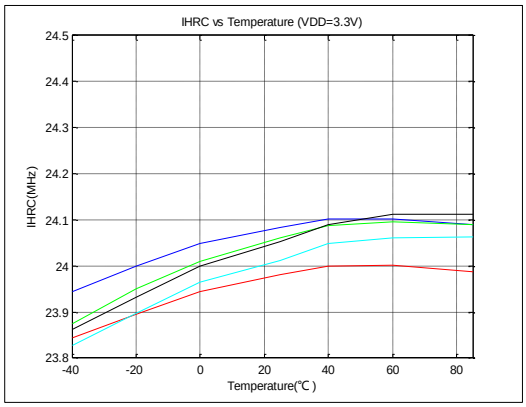


Figure 10. IHRC frequency vs temperature

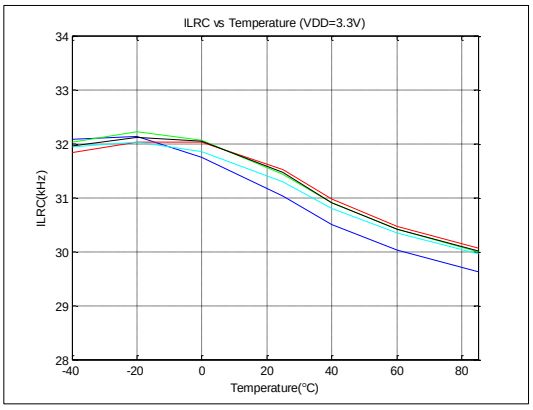


Figure 11. ILRC frequency vs temperature

Electrical Specifications

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	°C
T_S	Storage temperature	-55	+150	°C
VDD	Supply voltage	-0.2	+6.0	V
V_{IN}, V_{OUT}	Programming voltage	-0.2	VDD + 0.3	V
A_{IN}	Digital input/output voltage	-0.2	AVDDR + 0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		°C

Remarks:

1. CMOS device can be easily damaged by electrostatics. It must be stored in conductive foam and cannot exceed the operating voltage range.
2. Turn off power before inserting or removing the device.

Table 5. Electrical Specifications（VDD = 3.3V, T_A = 25°C）

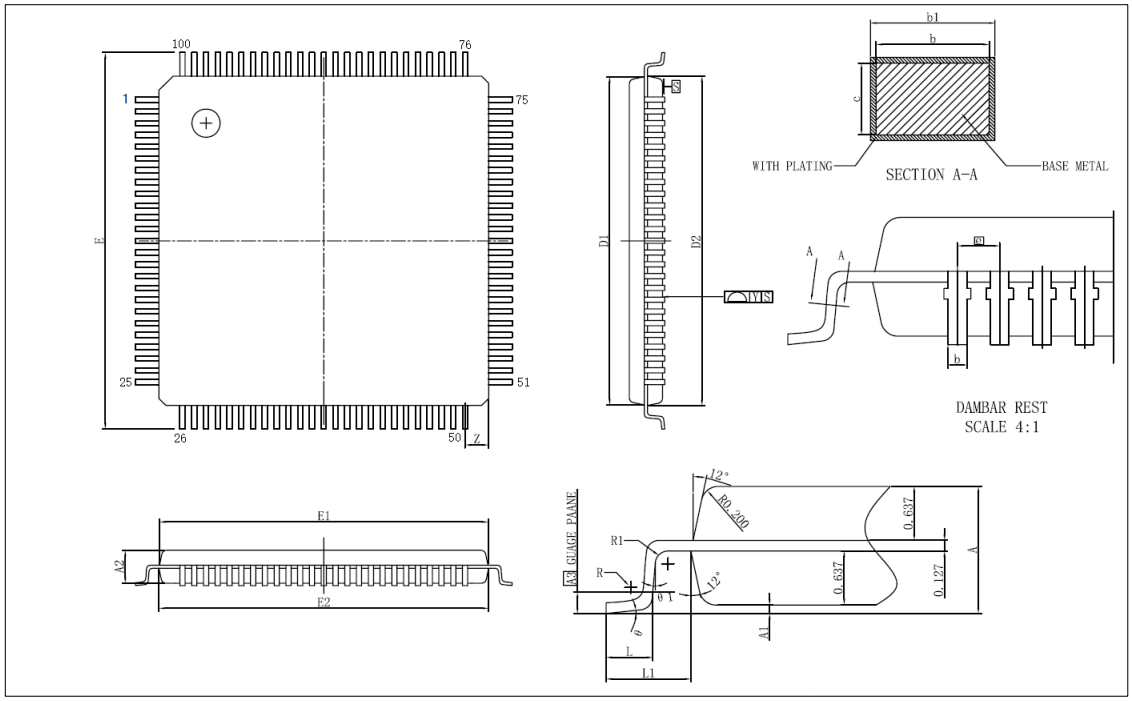
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4		5.5	V	Analog modules operating voltage
		1.35	1.5	1.65	V	Digital modules and MCU operating voltage
FOSC	Operating frequency	0.016	12	24	MHz	
IHRC	Internal high frequency RC oscillator	--	24	--	MHz	Frequency after calibration
ILRC	Internal low frequency RC oscillator	28	--	36	kHz	Frequency after calibration
IDD1	Operating current 1 (NORMAL mode)	--	4	--	mA	12MHz system clock. All modules are active without peripheral circuit (e.g. sensor, LCD display) connection
IDD2	Operating current 2 (WAIT mode)	--	1	--	mA	IDD1 type operation with CPU off
IDD3	Operating current 3 (DOZE mode)	--	5	--	μA	IDD1 type operation with CPU off, and modules with SYS_CLK, IHRC, and XTOSC2 as clock source are off
IDD4	Operating current 4 (STOP mode)	--	1.8	--	μA	IDD1 type operation with all clock sources off
Fsam	SDADC operating frequency	--	--	750	kHz	
OSR	Over sampling rate	128	--	16384		
NFbit	Noise free bits[1]	--	16	--	bits	Gain = 256 , input FSR = ±4mV
VINpga	PGIA differential input range[2]	-Vref[3]/Gain	--	Vref/Gain	mV	Gain = 1,4,8,16,32,64,128,256

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
Vavddr	AVDDR voltage output	--	2.4	--	V	AVDDRX [2:0] = 000
		--	2.7	--		AVDDRX [2:0] = 001
		--	3.0	--		AVDDRX [2:0] = 010
		--	3.3	--		AVDDRX [2:0] = 011
		--	3.6	--		AVDDRX [2:0] = 100
		--	3.9	--		AVDDRX [2:0] = 101
		--	4.2	--		AVDDRX [2:0] = 110
		--	4.5	--		AVDDRX [2:0] = 111
Iavddr	AVDDR current	--	10	--	mA	
POR	POR voltage	--	2.0	--	V	
LVD	LVD voltage	--	1.9	--	V	
THlbt	LVD hysteresis	--	200	--	mV	
Vlbt	Battery voltage detection	2.0	--	5.3	V	
VLCD	LCD driver output voltage	2.7	2.9	5.2	V	
Ilcd	LCD charge pump current [4]	--	--	500	μA	
Digital I/O parameter						
IOH	Output high current source	--	3	--	mA	VOH = VDD-0.3V , PTxSR = 0
		--	12	--		VOH = VDD-0.3V , PTxSR = 1
IOL	Output low current sink	--	3	--	mA	VOL = 0.3V , PTxSR = 0
		--	12	--		VOL = 0.3V , PTxSR = 1
VIH	Input high voltage	0.7VDD	--	--	V	
VIL	Input low voltage	--	--	0.3VDD	V	
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	
Rpu	Pin pull-up resistance	--	50	--	kΩ	VDD = 3.0

Notes:

1. Noise free bits and effective resolution are both related to the signal's full-scale range. Its peak to peak or rms noise plays the decisive role.
2. Two components that determine the ADC or PGIA input range are differential and absolute. The differential value is determined by PGIA gain and ADC voltage reference choice. The absolute value is limited by the circuit architecture.
3. The user can select either AVDDR or ACM as the originating source. The selected source is internally processed before becoming VREF.
4. The charge pump driving capability is related to the choice of capacitor and the operating frequency.

Packaging Information(SD93F115-JQS)

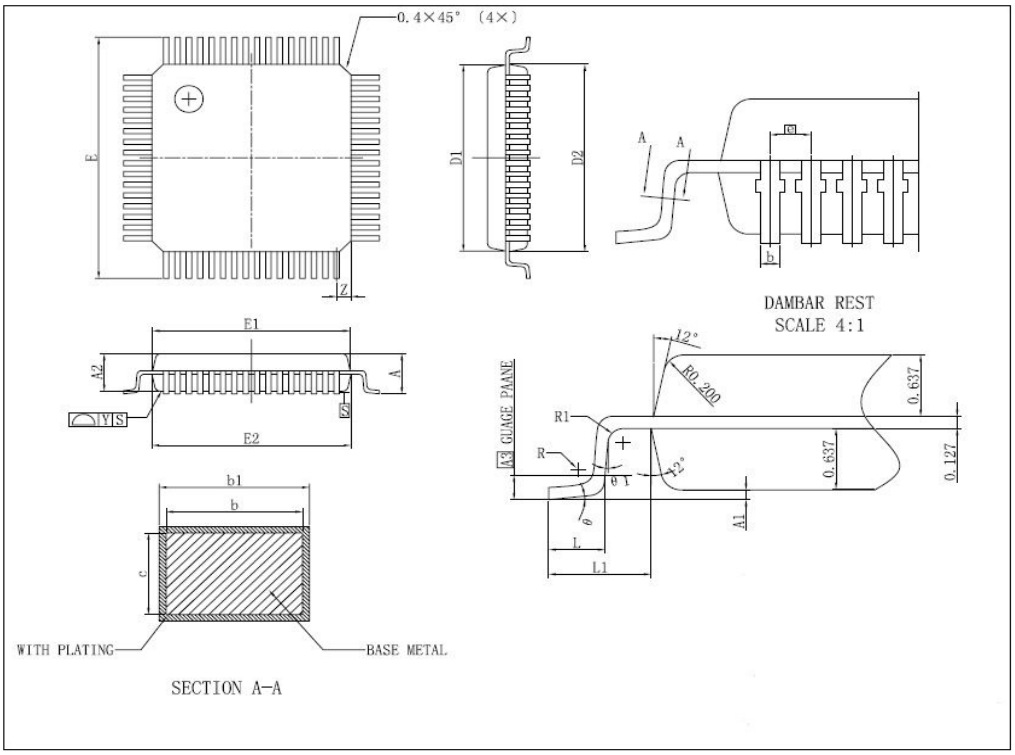


Dimensions: mm

Symbol	Min.	Nom.	Max.
A	1.45	1.55	1.65
A1	0.01	——	0.21
A2	1.30	1.40	1.50
A3	——	0.254	——
b	0.15	0.20	0.25
b1	0.16	0.22	0.28
c	——	0.127	——
D1	13.85	13.95	14.05
D2	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.85	13.95	14.05
E2	13.90	14.00	14.10
e	——	0.50	——
L	0.42	——	0.72
L1	0.95	1.00	1.15
R	0.10	——	0.25
R1	0.10	——	——
θ	0°	——	10°
θ1	0°	——	——

Figure 12. LQFP100 mechanical specification

LQFP64 Packaging Information (SD93F115-JBS)



Dimensions: mm

Symbol	Min.	Nom.	Max.
A	1.45	1.55	1.65
A1	0.01	---	0.21
A2	1.30	1.40	1.50
A3	---	0.254	---
b	0.13	0.18	0.23
b1	0.14	0.20	0.26
c	---	0.127	---
D1	6.85	6.95	7.05
D2	6.9	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10
e	---	0.4	---
L	0.43	---	0.71
L1	0.90	1.00	1.10
R	0.1	---	0.25
R1	0.1	---	---
θ	0	---	10°
θ1	0	---	---
y	---	---	0.1
z	---	0.5	---

Figure 13. LQFP64 mechanical specification